What is claimed is:

1. A circuit comprising:

a differential pair to receive a differential signal at a bulk input port and to generate an output signal at an output port.

2. The circuit of claim 1 further including a common gate of the differential pair to receive a gate bias voltage.

3. The circuit of claim 1 further including a common source/drain terminal of the differential pair coupled to a current source.

4. The circuit of claim 1 further including an amplifier coupled to the output port.

5. The circuit of claim 1 wherein the output signal is a function of the differential signal.

6. The circuit of claim 1 further including an active load coupled to the drain output port.

7. The circuit of claim 6 wherein the active load includes a transistor having a drain terminal shunted to a gate terminal.

8. The circuit of claim 6 wherein the active load includes a transistor.

9. The circuit of claim 6 wherein the active load includes a transistor having a bulk terminal coupled to a reference node.

10. The circuit of claim 6 wherein the active load includes a transistor pair having a common gate.

11. A circuit comprising:

a first transistor having a first bulk and a first drain;

a first input node at the first bulk; and

a first output node at the first drain.

12. The circuit of claim 11 further including a first gate of the first transistor to receive a bias voltage.

13. The circuit of claim 11 wherein the first transistor includes a first source to receive a bias current.

14. The circuit of claim 11 wherein the first transistor includes a first source coupled to a supply voltage.

15. The circuit of claim 11 further including a resistive load coupled to the first output node.

16. The circuit of claim 11 further including a second transistor having a second gate in common with the first gate, the second transistor having a second bulk and a second drain;

a second input node at the second bulk; and

a second output node at the second drain.

17. The circuit of claim 16 wherein the first transistor and the second transistor include a common source.

18. The circuit of claim 17 further including a current source coupled to the common source/drain.

19. A method comprising:

biasing a gate terminal of a first transistor in an amplifier;

providing an input signal to a bulk terminal of the first transistor; and

generating a first output signal as a function of the input signal at a first output terminal coupled to a first drain terminal of the amplifier.

20. The method of claim 19 wherein biasing includes providing a bias current.

21. The method of claim 19 wherein providing the input signal includes providing a first differential input signal to the first transistor of a differential pair and providing a second differential input signal to a second transistor of the differential pair.

22. The method of claim 21 further including generating a second output signal at a second output port coupled to a second drain terminal of the differential pair, the second output signal generated as a function of the first differential input signal and the second differential input signal.

23. The method of claim 21 further including biasing a source terminal of the first transistor.

24. The method of claim 23 wherein biasing the source terminal includes providing a current source.

25. The method of claim 21 wherein the first transistor is in a saturation mode.

26. A communication device comprising:

an antenna having an antenna output;

a first amplifier including a transistor having a bulk terminal coupled to the antenna output and a bias node coupled to a gate terminal of the transistor; and

a second amplifier having an input coupled to a first drain node of the first amplifier.

27. The device of claim 26 wherein the bulk terminal is coupled to the antenna output via a tuner.

28. The device of claim 26 further including a second source terminal of the transistor coupled to a power supply.

29. The device of claim 28 wherein the power supply includes a current source.

30. The device of claim 26 wherein the gate terminal is coupled to a voltage supply.

31. The device of claim 26 further including a resistor coupled to the first drain node and a reference node.

32. The device of claim 26 wherein the first amplifier includes a differential amplifier.

33. A system comprising:

a driver having a pair of differential output terminals;

a receiver having a pair of differential input terminals coupled to the pair of differential output terminals wherein each input terminal is coupled to a bulk terminal of a transistor.

34. The system of claim 33 wherein a gate terminal of each transistor is biased.

35. The system of claim 33 wherein the receiver includes an output terminal coupled to a drain terminal of the transistor.

36. The system of claim 33 wherein the transistor is biased in a saturation region.